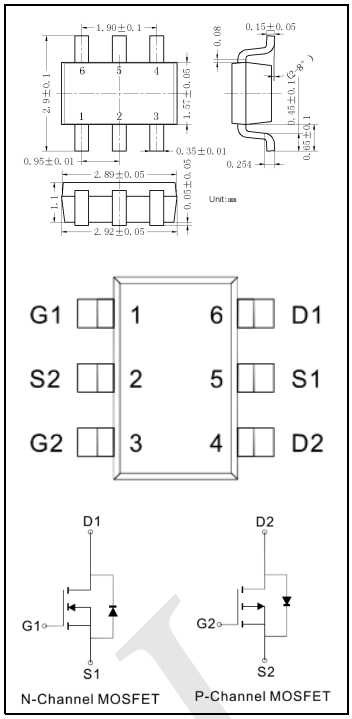
SHENZHEN LONG JING MICRO-ELECTRONICS CO., LTD.

SOT-23-6L Plastic-Encapsulate MOSFETS

LJ3587/LJ3587-G

N- and P-Channel 20V (D-S) MOSFET



Features

- $R_{DS(ON)}$ typ=37mΩ@V_{GS}=4.5V (N-Ch)
- $R_{DS(ON)}$ typ=42mΩ@V_{GS}=3.3V (N-Ch)
- $R_{DS(ON)}$ typ=52mΩ@V_{GS}=2.5V (N-Ch)
- $R_{DS(ON)}$ typ=83mΩ@V_{GS}=-4.5V (P-Ch)
- RDS(ON)typ =92mΩ@VGS=-3.3V (P-Ch)
- RDS(ON) typ=103mΩ@VGS=-2.5V (P-Ch)
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current

Applications

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC
- LCD Display inverter

General Description

The LJ3587 is the N- and P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high-density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where low in-line power loss are needed in a very small outline surface mount package.

Maximum Ratings (T_a=25°C unless otherwise specified)

Symbol	Parameter		Value				Unit
			N-channel		P-channel		
V_{DS}	Drain-Source voltage		20		-20		V
V_{GS}	Gate-Source voltage		±8		±8		
I_D	Continuous Drain Current *	T_A = 25 °C	4.6		-3.1		A
		T_A = 70 °C	3.2		-2.5		
I_{DM}	Pulsed Drain Current		16		-10		
P_D	Maximum Power Dissipation	T_A = 25 °C	1.18		1.18		W
		T_A = 70 °C	0.75		0.75		
T_J	Operating Junction Temperature		-55 to +150		-55 to +150		°C
$R_{\theta JA}$	Maximum Junction-to-Ambient*		Typical	Maximum	Typical	Maximum	°C/W
			106	150	100	150	

* The device mounted on 1in^2 FR4 board with 2 oz copper

N-Channel Electrical Characteristics (T_A=25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Static						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	20			V
$V_{GS(th)}$	Gate-Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	0.5		1.2	V
I_{GSS}	Gate-body Leakage current	V_{DS} = 0V, V_{GS} = ±8V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 20V, V_{GS} = 0V			1	μA
$R_{DS(on)}$	Drain-Source On-Resistance [1]	V_{GS} = 4.5V, I_D = 3.4A		37	45	mΩ
		V_{GS}		42	48	
		V_{GS} = 2.5V, I_D = 3A		52	62	
		V_{GS} = 1.8V, I_D = 2A		92	120	
V_{SD}	Diode Forward Voltage	I_S = 1A, V_{GS} = 0V		0.7		V
Dynamic						
Q_g	Total Gate Charge	V_{GS} = 4.5V,		5.3		nC
Q_{gs}	Gate-Source Charge	I_D = 2.1A,		1.7		
Q_{gd}	Gate-Drain Charge	V_{DS} = 15V		1.4		
C_{iss}	Input Capacitance	V_{GS} = 0V		340		pF
C_{oss}	Output Capacitance	V_{DS} = 15V		50		
C_{rss}	Reverse Transfer Capacitance	f = 1.0MHz		15		
$t_{d(on)}$	Turn-On Delay Time	V_{DS} = 10V, R_L = 10Ω		4		ns
t_r	Rise Time	R_{GEN} = 3Ω, V_{GS} = 5V		14		
$t_{d(off)}$	Turn-Off Delay Time			21		
t_f	Fall Time			5		

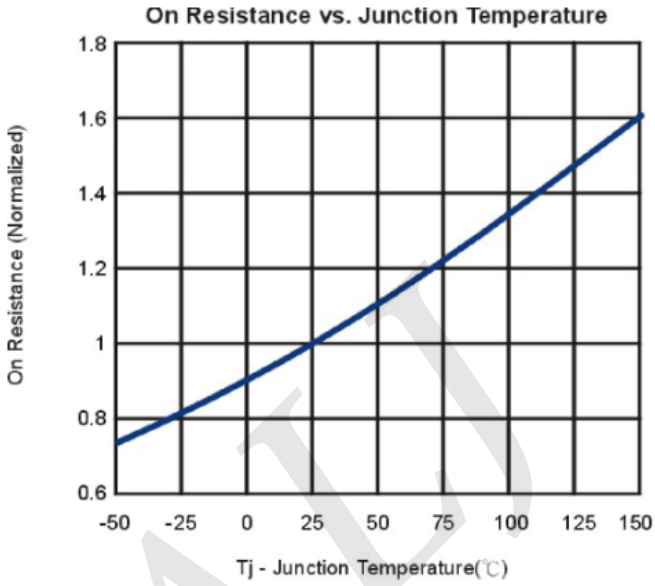
P-Channel Electrical Characteristics (T_A=25°C unless otherwise specified)

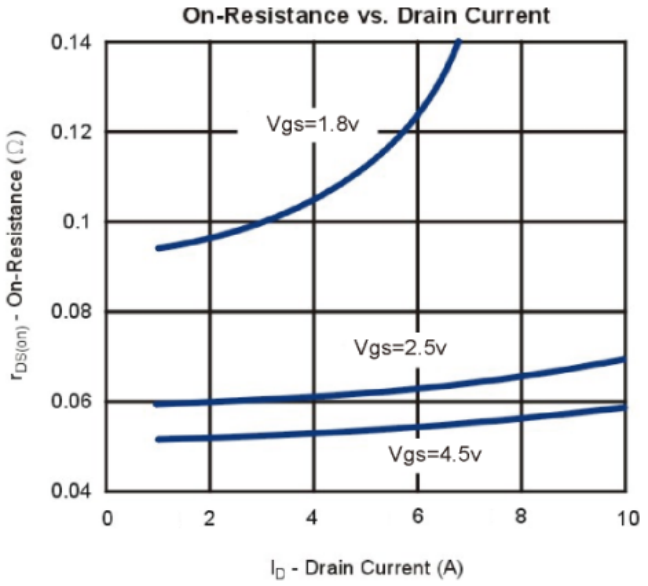
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Static						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = -250μA	-20			V
$V_{GS(th)}$	Gate-Threshold Voltage	V_{DS} = V_{GS}, I_D = -250μA	-0.4		-1	V
I_{GSS}	Gate-body Leakage current	V_{DS} = 0V, V_{GS} = ±8V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -20V, V_{GS} = 0V			-1	μA
$R_{DS(on)}$	Drain-Source On-Resistance [1]	V_{GS} = -4.5V, I_D = -2.8A		83	100	mΩ
		V_{GS} = -3.3V, I_D = -2A		92	110	
		V_{GS} = -2.5V, I_D = -2A		103	123	
		V_{GS} = -1.8V, I_D = -1A		130	160	
V_{SD}	Diode Forward Voltage	I_S = -1A, V_{GS} = 0V		-0.7	-1.4	V
Dynamic						
Q_g	Total Gate Charge	V_{GS} =-4.5V,		7.2		nC
Q_{gs}	Gate-Source Charge	I_D = -2.1A,		2.2		
Q_{gd}	Gate-Drain Charge	V_{DS} = -15V		1.2		
C_{iss}	Input Capacitance	V_{GS} = 0V		480		pF
C_{oss}	Output Capacitance	V_{DS} = -15V		46		
C_{rss}	Reverse Transfer Capacitance	f = 1.0MHz		10		
$t_{d(on)}$	Turn-On Delay Time	V_{DS} = -6V, R_L =6Ω		6		ns
t_r	Rise Time	R_{GEN} =6Ω, V_{GS} = -4.5V		14		
$t_{d(off)}$	Turn-Off Delay Time			27		
t_f	Fall Time			5		

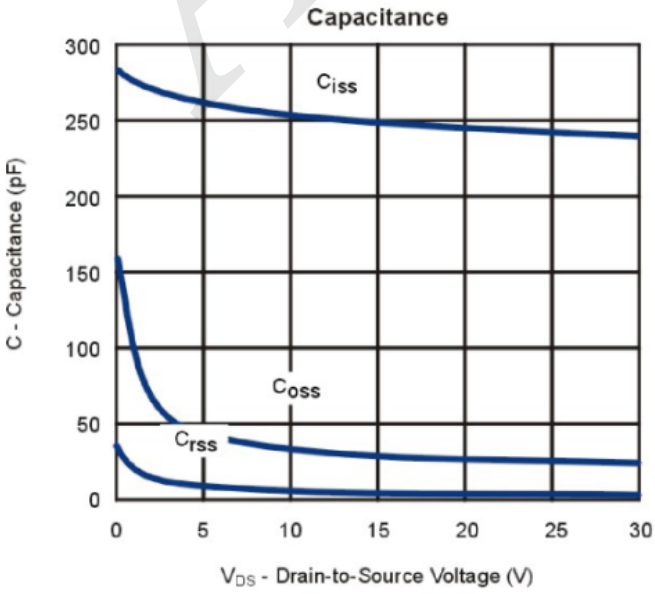
Notes

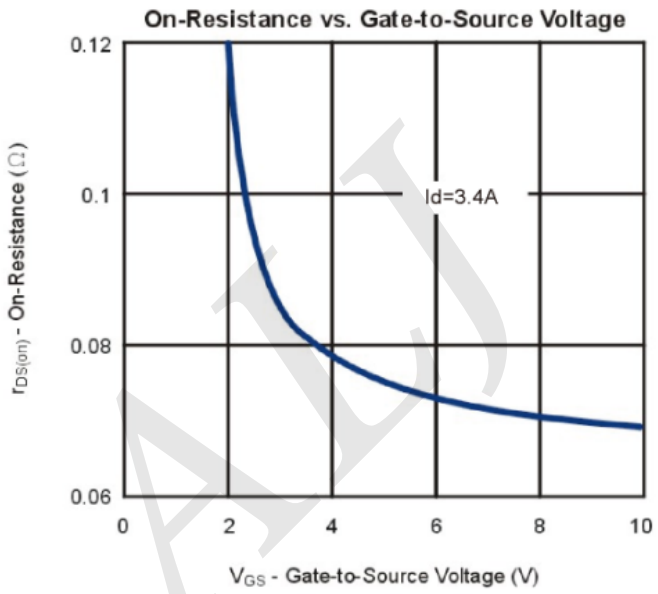
1. Pulse test; pulse width ≦ 300us, duty cycle≦ 2%

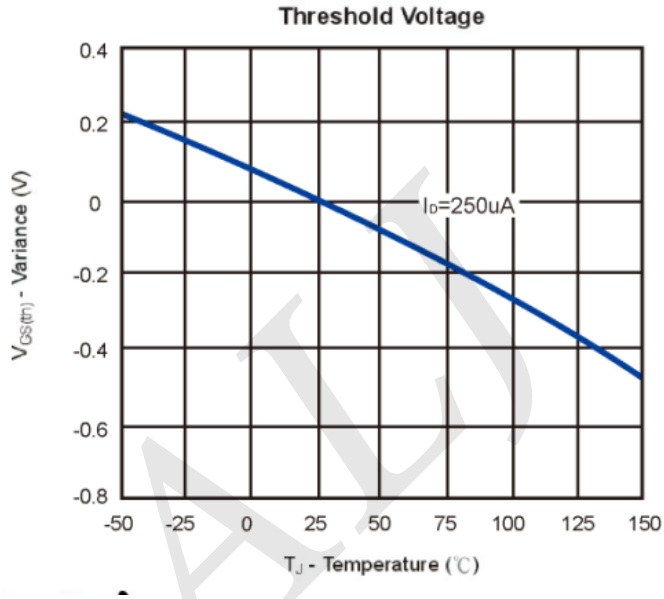
N-Channel Typical Characteristics

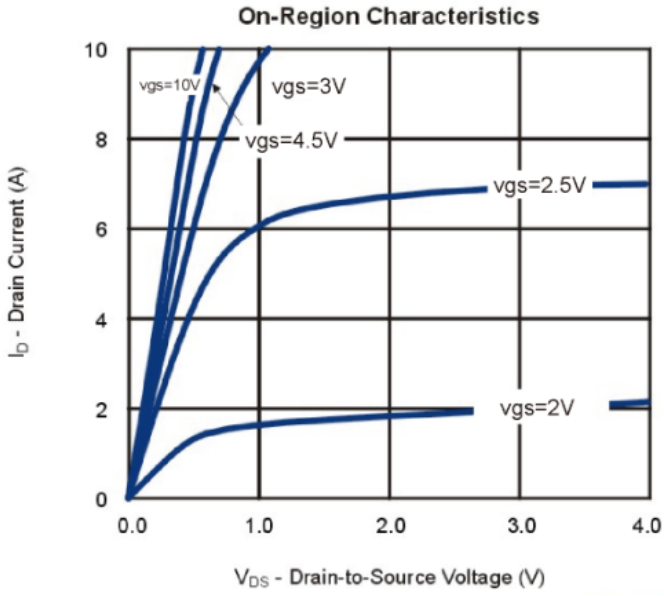






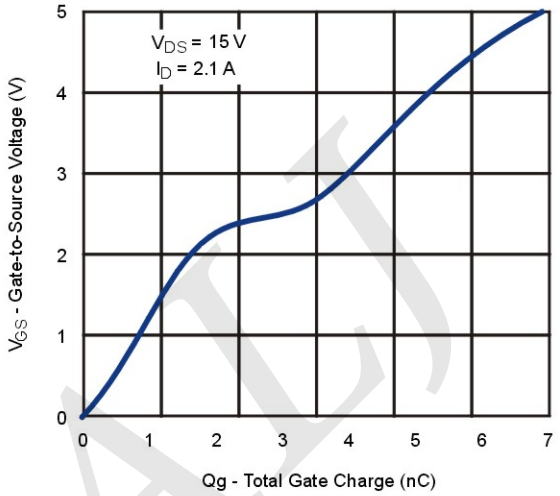




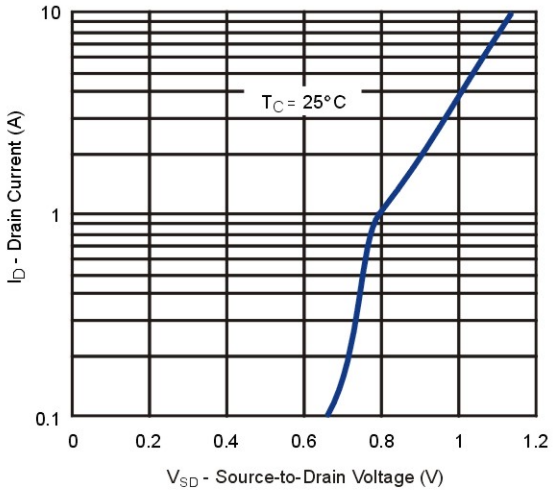


N-Channel Typical Characteristics (Cont.)

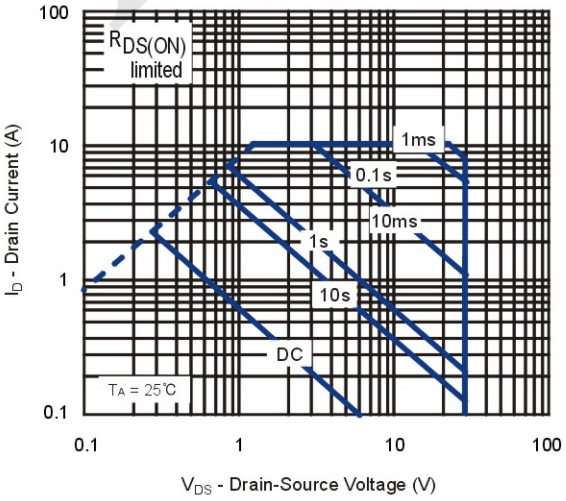
Gate Charge



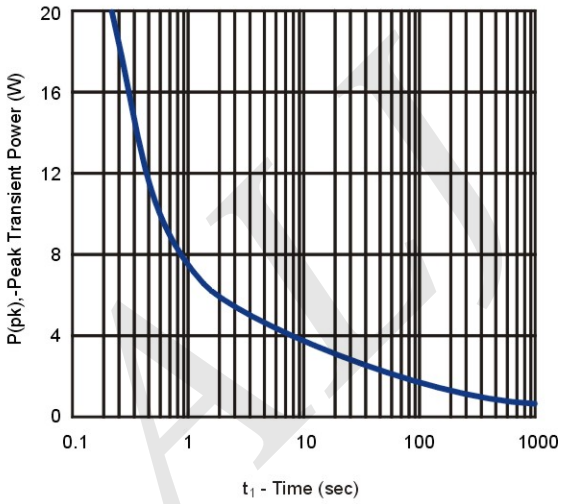
Body - Diode Characteristics



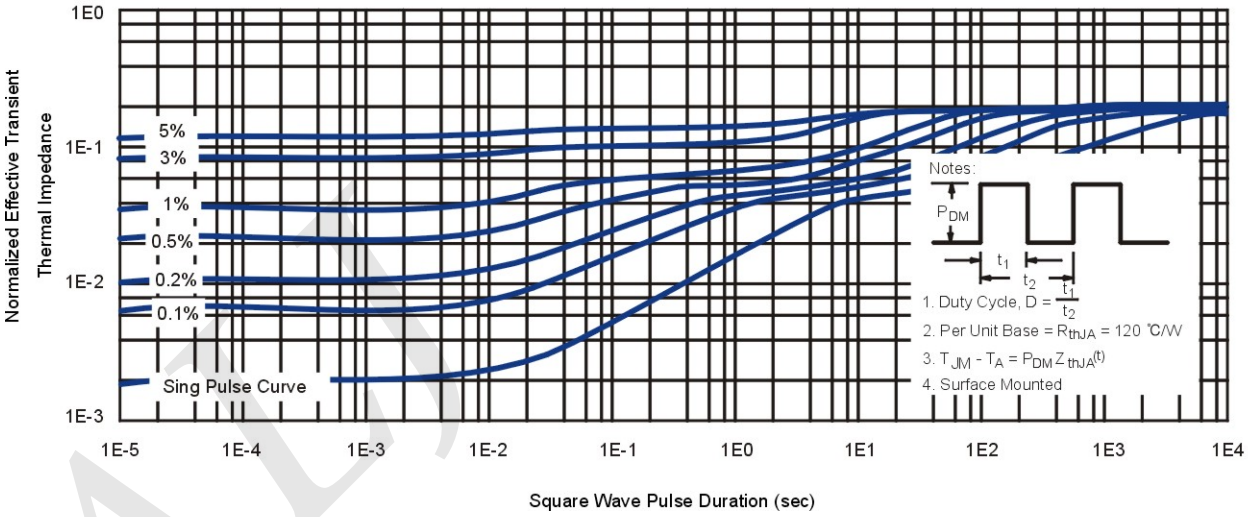
Maximum Forward Biased Safe Operating Area



Single Pulse Maximum Power Dissipation

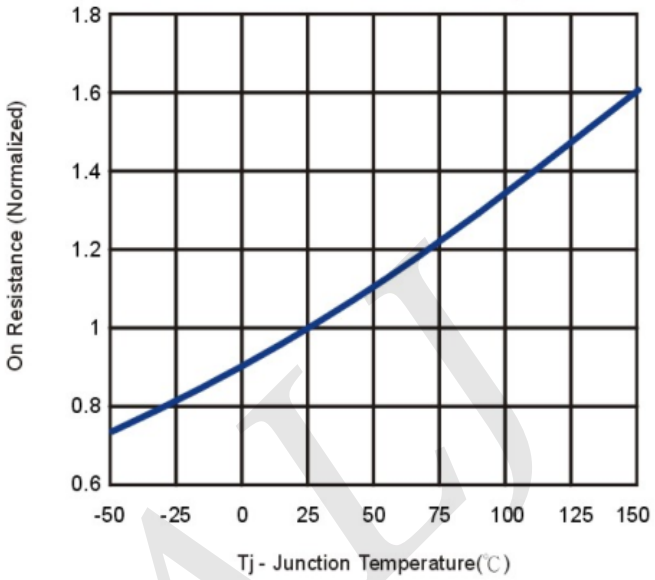


Normalized Thermal Transient Impedance, Junction-to-Ambient

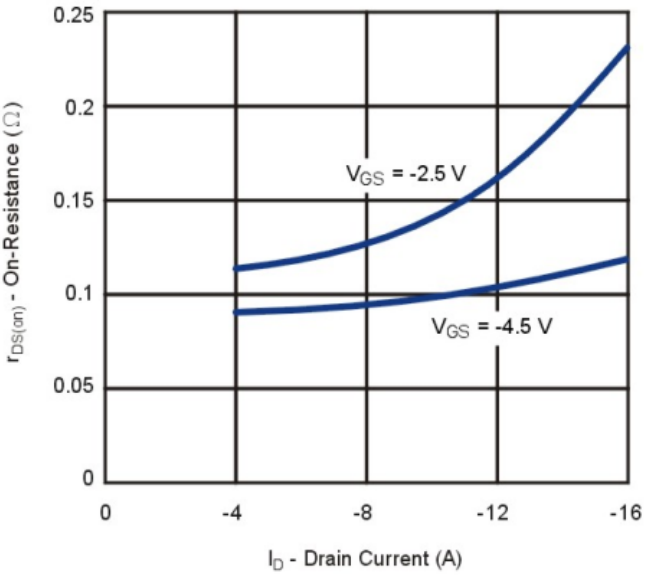


P-Channel Typical Characteristics

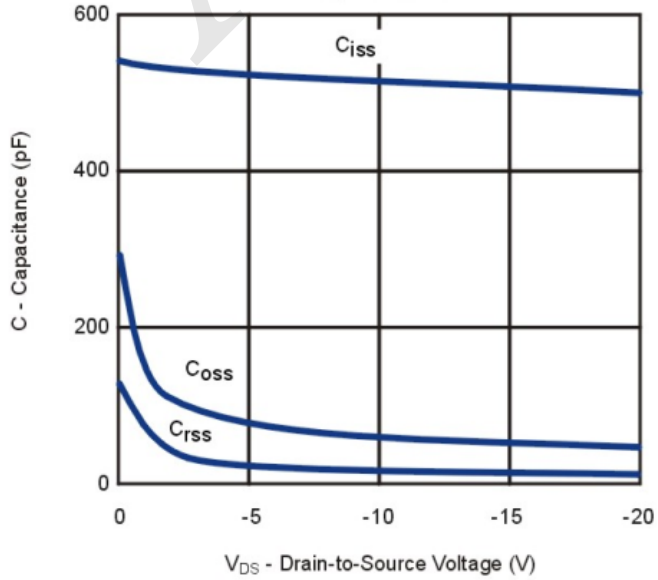
On Resistance vs. Junction Temperature



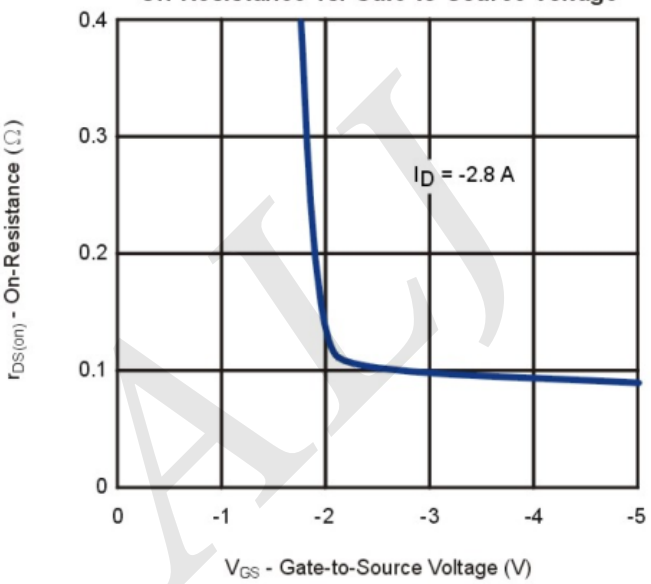
On-Resistance vs. Drain Current



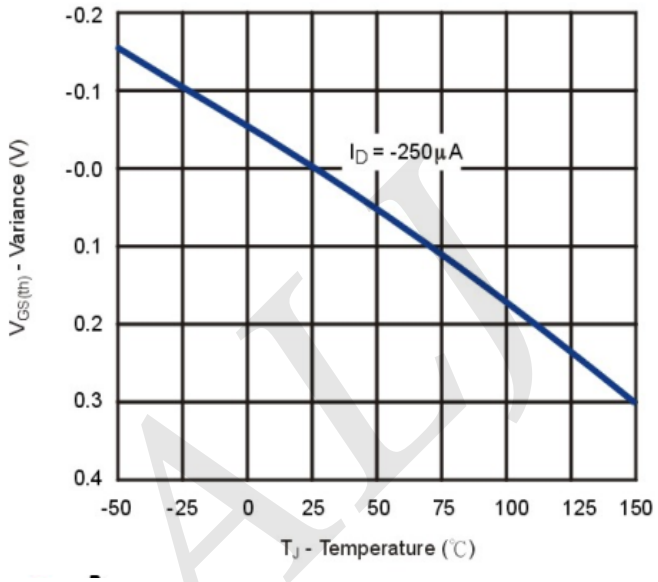
Capacitance



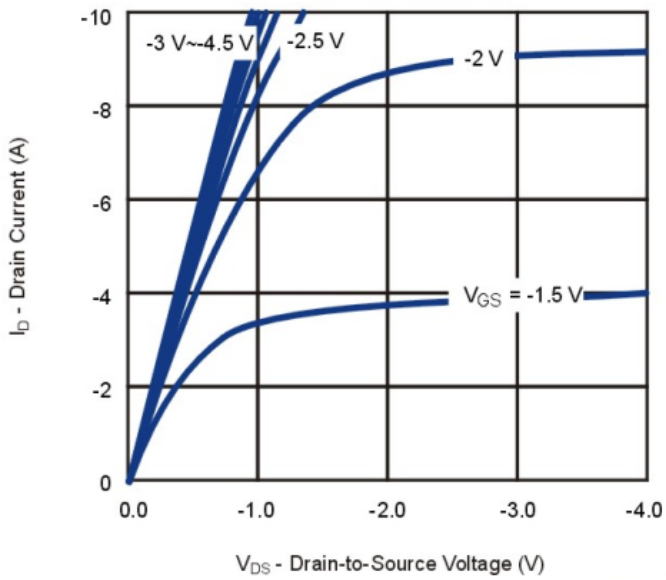
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

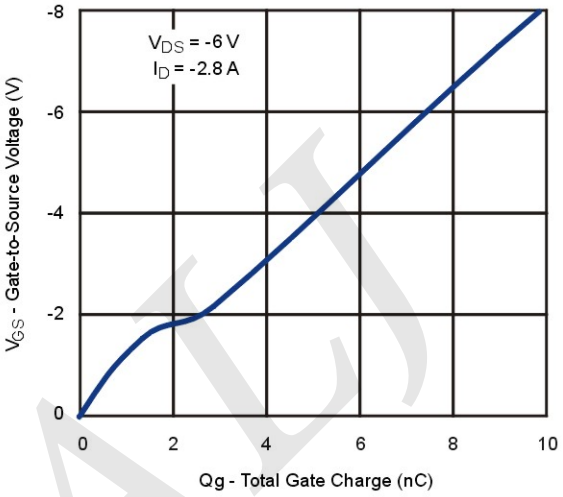


On-Region Characteristics

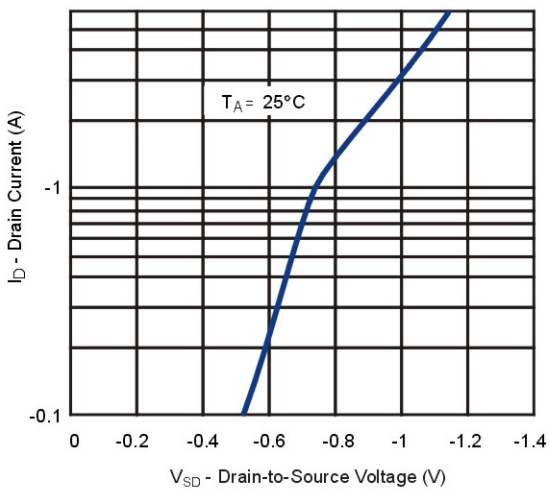


P-Channel Typical Characteristics (Cont.)

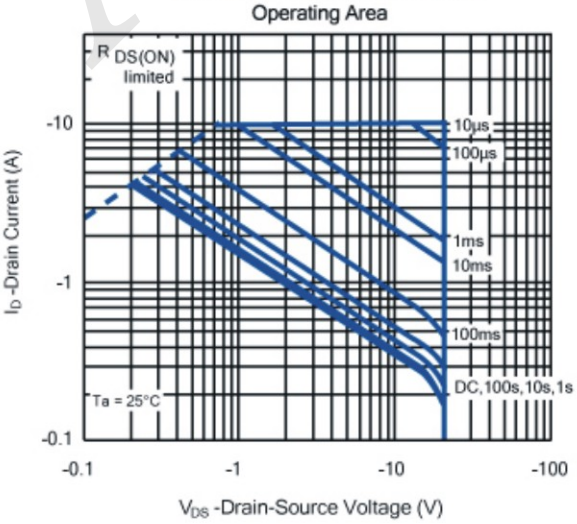
Gate Charge



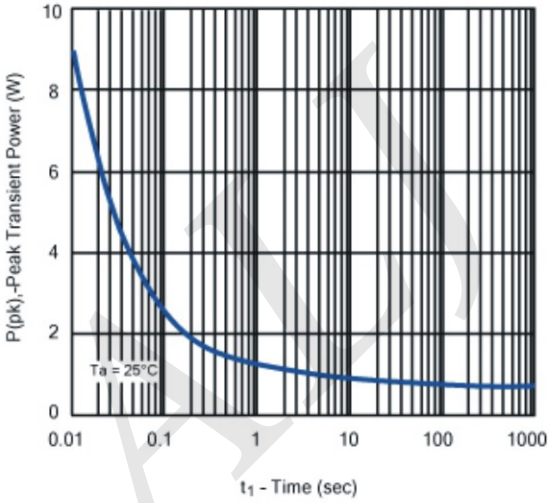
On-Resistance vs. Drain Current



Maximum Forward Biased Safe Operating Area



Single Pulse Maximum Power Dissipation



Normalized Thermal Transient Impedance, Junction-to-Ambient