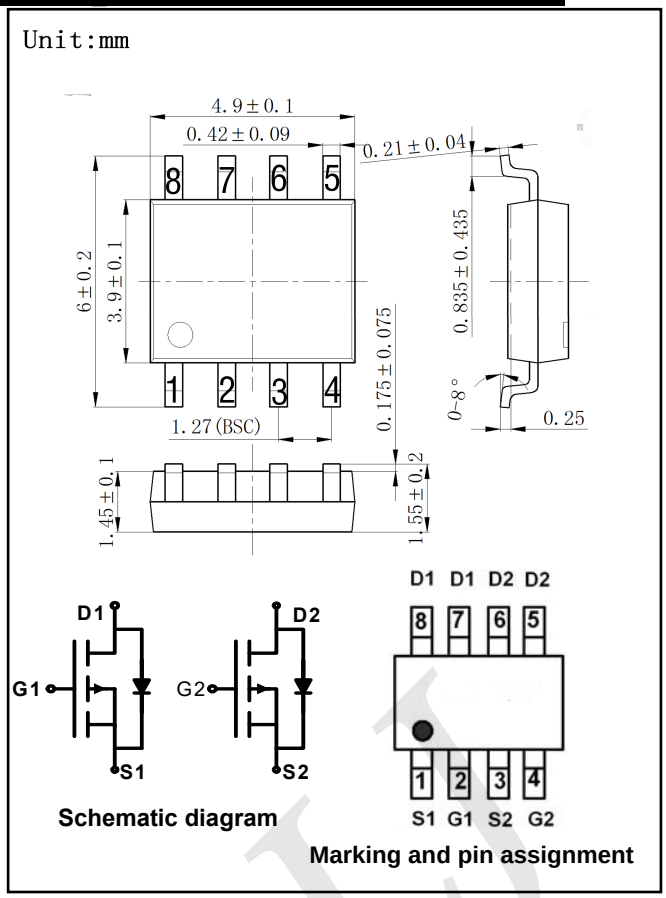
SOP-8L Plastic-Encapsulate MOSFETS

ALJ55P04S

P-Channel enhancement mode power mosfet



Schematic diagram

Marking and pin assignment

Description

The ALJ55P04S uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

Features

- V_{DS} =-55V,I_D =-4A
  $R_{DS(ON)}$ <82mΩ @ V_{GS}=-10V
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

Application

- Power switching application
- Hard switched and high frequency circuits
- DC-DC Converter

Absolute Maximum Ratings

Symbol	Parameter		Limit	Unit
I_D	Drain Current	Ta=25°C	-4	A
I_D	Drain Current-Continuous (Tc=100°C)		-2.8	
I_{DM}	Pulsed Drain Current		-25	
P_D	Max Power Dissipation	Ta=25°C	3	W
V_{GS}	Gate-to-Source Voltage		±20	V
V_{DS}	Drain-Source Voltage		-55	
T_{STG}	Storage Temperature Range		-55 to + 150	°C
T_J	Junction Temperature			

Thermal Resistance

Symbol	Parameter	Limit	Unit
$R_{\theta JA}$	Thermal Resistance.Junction- to-Ambient(note 2)	42	°C/W

Electrical Characteristics (T_J=25°C unless otherwise specified)

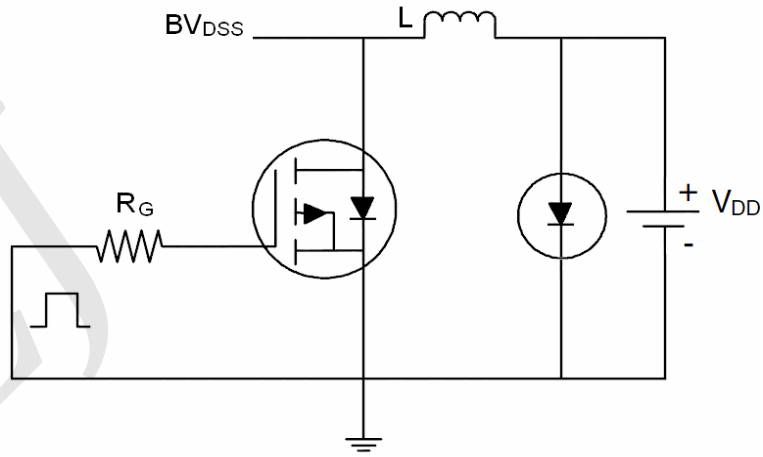
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	V_{GS} = 0V, I_D = -250μA	-55			V
$R_{DS(On)}$	Static Drain-Source On-Resistance[2]	V_{GS} =-10V, I_D = -4A		66	82	mΩ
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = -250μA	-1.5	-2.6	-3.5	V
I_{DSS}	Drain-to-Source leakage current	V_{DS} =-55V, V_{GS} = 0V			-1	uA
I_{GSS}	Gate-to-Source forward leakage	V_{GS} = 20V, V_{DS}=0V			100	nA
	Gate-to-Source reverse leakage	V_{GS} = -20V, V_{DS}=0V			-100	
g_{fs}	Forward Transconductance	V_{DS}=-15V, I_D=-4A	16			S
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=-30V, R_L=30Ω V_{GS}=-10V,R_{GEN}=6Ω		8		ns
tr	Turn-On Rise Time			9		
$t_{d(off)}$	Turn-Off Delay Time			65		
tf	Turn-Off Fall Time			30		
C_{iss}	Input Capacitance	V_{GS} = 0V V_{DS} = -25V f = 1.0MHz		1450		pF
C_{oss}	Output Capacitance			145		
C_{rss}	Reverse Transfer Capacitance			110		
Q_g	Total Gate Charge	V_{DS} = -30 V, V_{GS} = -10 V, I_D = -4 A		26		nC
Q_{gs}	Gate Source Charge			4.5		
Q_{gd}	Gate Drain Charge			7		
V_{SD}	Diode Forward Voltage(note3)	I_S=-4A, V_{GS}=0V			-1.2	V
I_S	Diode Forward Current (Note 2)				-4	A

Notes :

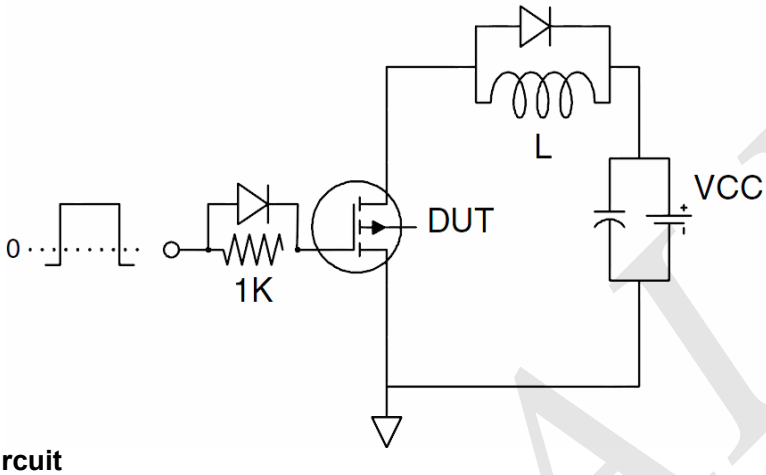
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production.

Test Circuit

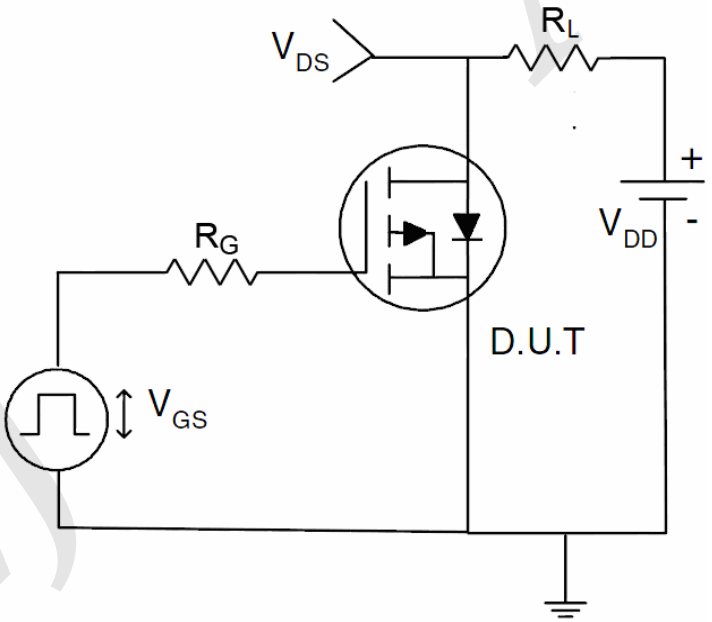
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Characteristics

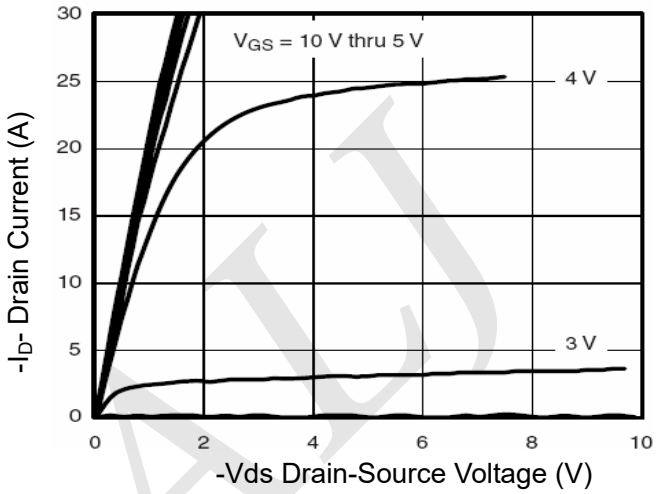


Figure 1 Output Characteristics

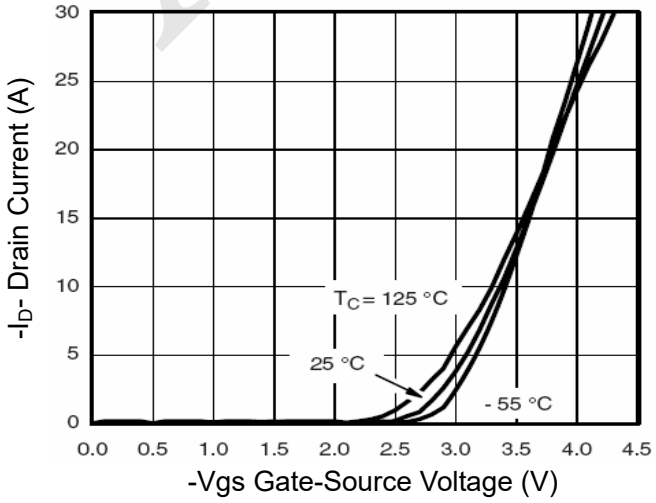


Figure 2 Transfer Characteristics

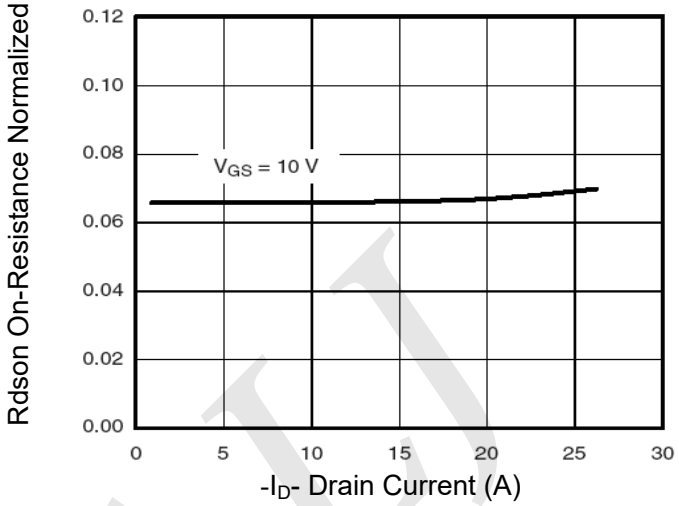


Figure 3 Rdson- Drain Current

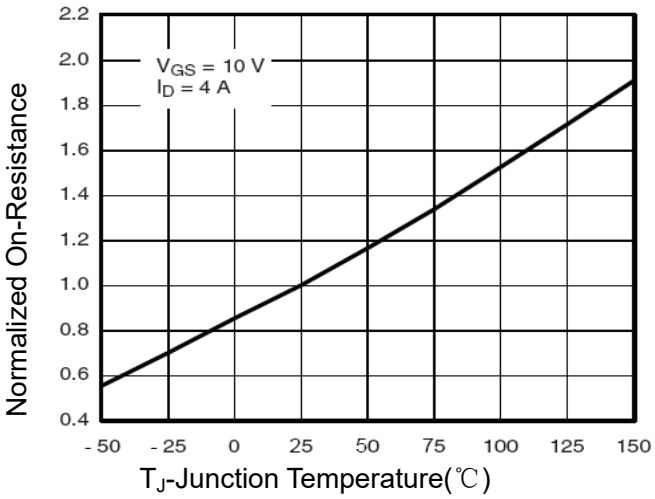


Figure 4 Rdson-Junction Temperature

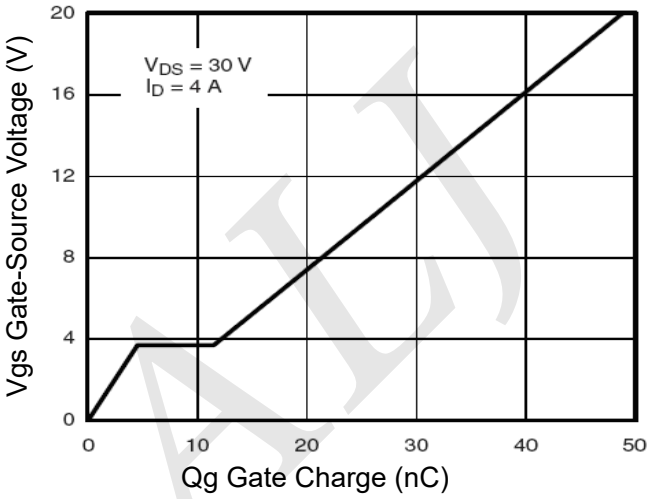


Figure 5 Gate Charge

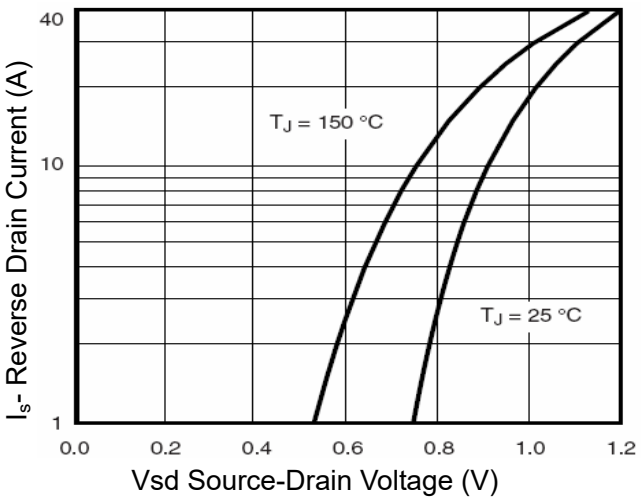


Figure 6 Source- Drain Diode Forward

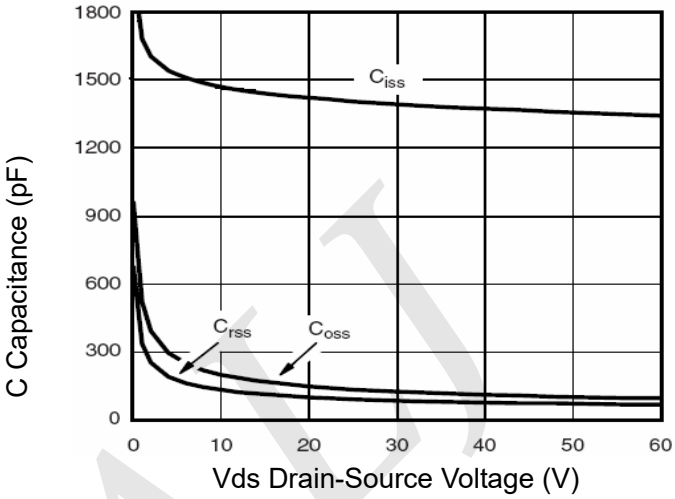


Figure 7 Capacitance vs Vds

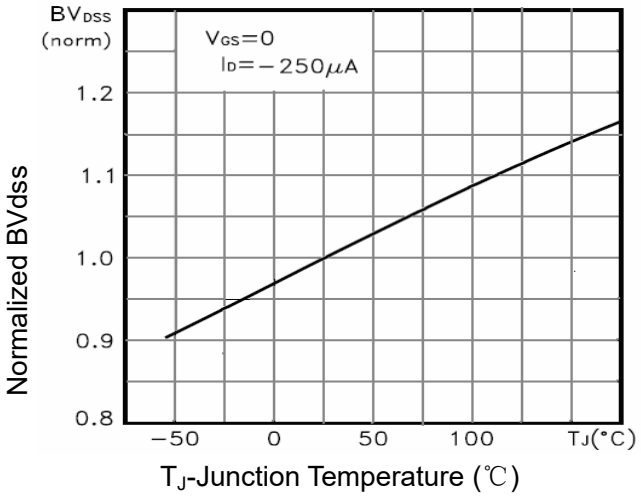


Figure 9 BV_{DSS} vs Junction Temperature

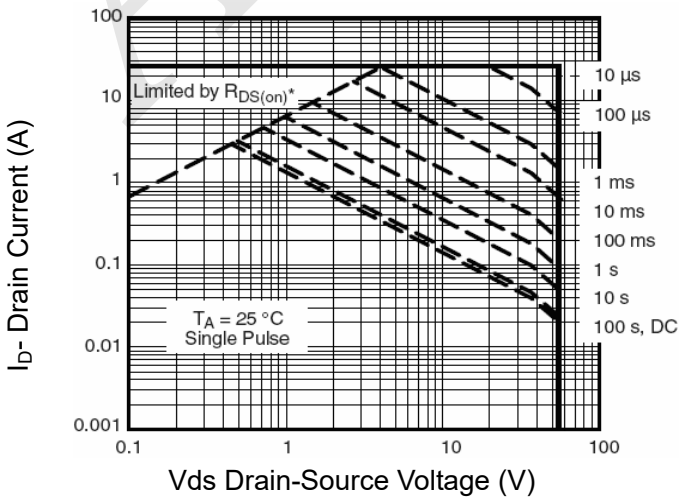


Figure 8 Safe Operation Area

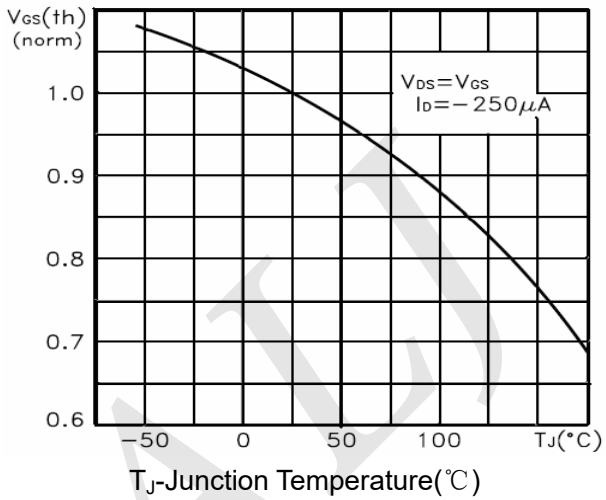


Figure 10 $V_{GS(th)}$ vs Junction Temperature

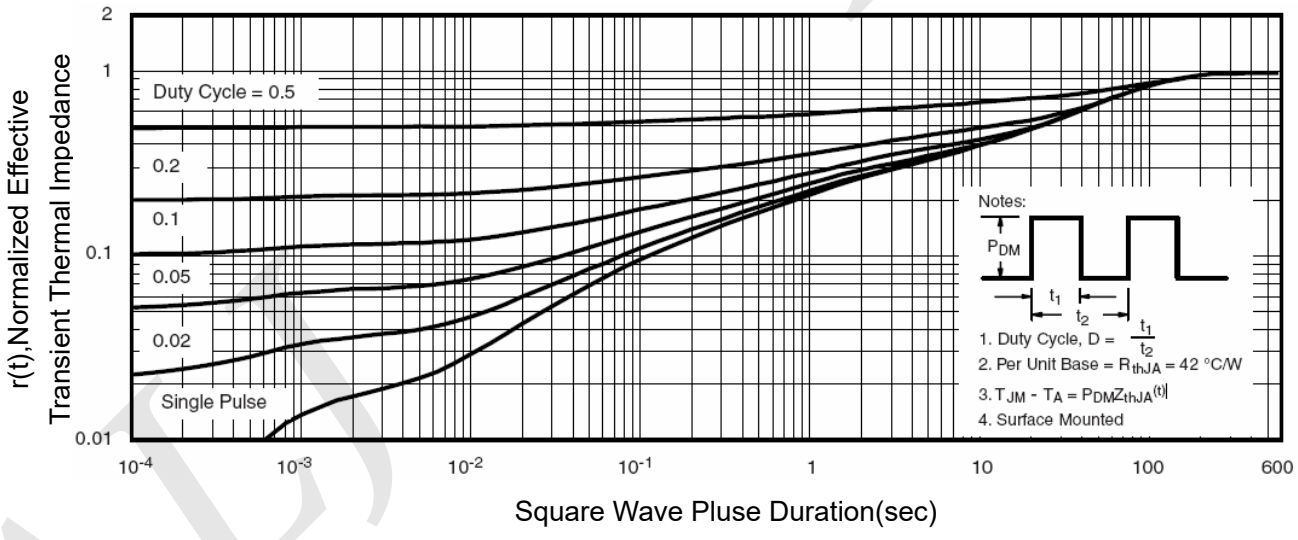


Figure 11 Normalized Maximum Transient Thermal Impedance